REMARKS

The application as originally filed included claims nos. 1-20. Paragraphs 0011, 0012, 0036, and 0040 have been amended to correct the errors noted by the Examiner. Claims 1, 4, 7, and 16 have been amended. No new matter has been added. Applicants request favorable consideration in light of the above amendments and following remarks.

Objections to the Specification

The objections to specification have been obviated by amendment.

35 U.S.C. § 112

Objections to claims 1-9 and 16-20 have been obviated by amendment.

35 U.S.C. § 102

Claims 16-19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent 6,114,243 to *Gupta et al.* and under 35 U.S.C. § 102(e) as being anticipated by US Patent 6,818,557 to *Ngo et al.* Applicants respectfully submit that claims 16-19 recite limitations that are not disclosed by *Gupta* or *Ngo*, either singly or in combination

Independent claim 16

Independent claim 16 is directed to a method for removal of chemical residues from a surface. The surface from which the residue is removed has a metal pattern formed in a dielectric substrate by a Chemical Mechanical Polishing (CMP) process. In the method, the surface is plasma etched to remove "at least a thickness of the metal material corresponding to a thickness of metal residue formed by the CMP process." Accordingly, claim 16 recites

removing metal residue formed in a dielectric subtract by a CMP process by plasma etching the surface to remove the metal residue from the surface.

Gupta

The cited reference to *Gupta*, on the other hand, relates to prevention of copper contamination of an intermetal dielectric layer during via or dual damascene etching by forming a capping layer over a first metallization. (*Gupta*, Abstract). In *Gupta*, a barrier metal layer is formed over an IMD or ILD layer and within openings in the IMD or ILD. (col. 3, ll. 18-21). The barrier metal layer is a polish stop layer for a CMP process. (col. 3, ll. 31-32). A copper layer is formed over the barrier metal layer, and excess copper is polished off by the CMP process (col. 3, ll. 29-31). The copper layer in the trench is stripped, and a capping layer is formed over the copper layer. (col. 3, ll. 36-44).

In all embodiments described by *Gupta*, a metal layer that is formed over the barrier metal layer is stripped back to form a recess (A) in the trench and a capping layer is formed over the metallization to prevent contamination before the next level of metallization. (col. 3, ll. 43-45). In *Gupta,* the capping layer is removed, while leaving the capping in the trench. (col. 3, ll. 47-50). In the first embodiment, a spin-on material coated over the barrier metal layer and field is etched back, leaving a layer of spin on material and conductive cap over metal trenches (col. 4, 36-37). In the second embodiment, the substrate and trench are coated with a photoresist mask, and the conductive cap layer not covered by the mask is etched using Cl or F plasma (col. 4, ll. 54-64). Finally, in the third embodiment, the IMD or ILD is coated with capping material and a partial CMP is performed to partially remove the capping material followed by a blanket etch back of the conductive cap layer using a Cl or F plasma

to remove the capping material above the trench and field areas so that the conductive cap remains only above the trenches. (col. 5, ll. 10-22). Only in the third embodiment is a CMP process performed, and that CMP process includes only partial removal of only the metal barrier.

Ngo

Ngo relates to electromigration resistance of capped Cu or Cu alloy interconnects where an exposed planarized surface of in-laid Cu is sequentially and contiguously treated with plasma containing NH_3 and N_2, while trimethylsilane (TMS) is increasingly introducing and then deposition of a silicon carbide capping layer is initiated. (*Ngo*, Abstract). A thin film of oxide 20 is formed on the exposed surface of the Cu interconnect 13A as the result of a CMP process to remove portions of Cu that extend beyond the trench. (col. 7, l. 65 to col. 8, l. 1). The copper interconnect with the exposed oxide is treated with a soft plasma to remove or reduce the oxide film to leave a clean sensitized and highly reactive Cu surface 30. (col. 8, ll. 5-11). The power is removed, TMS is slowly introduced and a plasma re-introduced to deposit a silicon carbide capping layer on the clean exposed surface of the copper interconnect. Accordingly, in *Ngo*, an oxide that is formed over a Cu interconnect is treated with a plasma to remove the oxide and then again to deposit a silicon carbide capping.

Neither *Gupta* nor *Ngo* Disclose Limitations of Claim 16

Applicants respectfully submit that *Gupta* and *Ngo* do not disclose the limitations of claim 16. In particular, neither *Gupta* nor *Ngo* disclose removal of metal residue formed in a dielectric by the CMP process.

In *Gupta*, a CMP process is used to remove a barrier metal in the field. The barrier metal is coated in the field before the CMP process and the CMP is used to partially remove the barrier. A blanket etch back is performed to remove the remainder of the barrier. In none of the embodiments of *Gupta* includes a CMP process that may form a metal residue in a dielectric. To the contrary, *Gupta* describes using a CMP process to remove material in the field. Indeed, *Gupta* describes using the barrier metal as a polish stop layer for the CMP process. (col. 3, ll. 31-32). To the extent that *Gupta* describes plasma etching, that etching is performed to remove material that is deposited on the layer and not formed as the result of a CMP process as claim 16. Because *Gupta* does not disclose plasma etching a surface to remove metal residue formed in a dielectric substrate by a CMP process, limitations of claim 16 are not disclosed by *Gupta*. Applicants respectfully request reconsideration of the rejection of claim 16.

In *Ngo*, a plasma is used to remove an oxide that is formed over a Cu interconnect and to deposit a silicon carbide capping. *Ngo* does not describe that a metal residue in a dielectric substrate may be formed by the CMP process. Rather, in *Ngo* an oxide over metal is formed by a CMP process (col. 5, ll. 50-52). That oxide, not the underlying metal, is removed using soft plasma. Nowhere in the specification does *Ngo* describe that a metal

residue formed in the dielectric substrate is removed. Because *Ngo* does not disclose plasma etching a surface to remove metal residue formed in a dielectric substrate by a CMP process, limitations of claim 16 are not disclosed by *Ngo*. Applicants respectfully request reconsideration of the rejection of claim 16.

Dependent Claims

For similar reasons, *Gupta* and *Ngo* also fail to disclose the limitations of claims 17-19. As discussed above, *Gupta* and *Ngo* do not disclose the limitations for independent claim 16. Therefore, *Gupta* and *Ngo* also do not disclose the limitations for claims dependent therefrom. Accordingly, Applicants also respectfully request favorable consideration of claims 17-19.

35 U.S.C. § 103

Claims 1-15 have been rejected under 35 U.S.C. § 103(a) as being obvious over *Ngo* in view of Published US Patent Application No. US 2004/0248409 to *Padhi et al.* and in further view of *Gupta*. Applicants respectfully submit that claims 1-15 recite limitations that are not disclosed or fairly suggested by the *Ngo*, *Padhi* and *Gupta* combination.

Independent claim 1

Independent claim 1 is directed to a method for dry-cleaning residue from a semiconductor surface. In the method, a metal trench pattern of conductive metal is formed in a dielectric layer of a semiconductor device. The conductive metal and the dielectric layer define a semiconductor surface that is prepared using a chemical mechanical polish (CMP) process. The metal residue that is dry-cleaned includes the conductive metal that is smeared

in an unintended scratch at the semiconductor surface. The prepared semiconductor surface is exposed to plasma and an inert gas, having ions reacting with the metal residue to form a volatile gas. The prepared semiconductor surface is exposed to the plasma for a predetermined range of time to remove the metal residue from the scratch. Therefore, in the method of claim 1, the metal in a trench pattern that is smeared in a scratch of a dielectric surface is removed.

Ngo

As discussed, *Ngo* relates to electromigration resistance of capped Cu or Cu alloy interconnects where an exposed planarized surface of in-laid Cu is sequentially and contiguously treated with plasma containing NH_3 and N_2, while TMS is increasingly introducing and then deposition of a silicon carbide capping layer is initiated. (*Ngo*, Abstract). In *Ngo*, an oxide that is formed over a Cu interconnect, not a metal residue, is removed. Moreover, in *Ngo*, plasma is used to remove the oxide and to deposit a silicon carbide capping over a trench.

Padhi

In the *Padhi*, a protective layer is deposited on the surface of a semiconductor substrate having a conductive element. (Abstract). The protective layer is processed to expose the conductive element and a metallic passivating layer is deposited onto the conductive element. *Padhi* describes that CMP techniques may be used to polish away unwanted conductive metal and to prepare the substrate for deposition of the passivating layer. (par. [0062]). Indeed, *Padhi* describes that "CMP is suitable for removal of various materials, including metals and dielectric materials," and that other treatments that "include

cleaning with an acidic solution" are used "to remove metal oxides and other contaminants from the substrate surface. (par. [0063]). Finally, *Padhi* discusses that the exposed conductive feature can also be rinsed with distilled water to remove residual contaminants from the surface treatment process. *Id.* Accordingly, *Padhi* discloses using CMP to remove metal from the substrate surface and subsequently using wet etching techniques to remove oxides and other residues.

Gupta

As discussed, *Gupta* prevents copper contamination of an intermetal dielectric layer during via or dual damascene etching by forming a capping layer over a first metallization. (*Gupta*, Abstract). In all embodiments of *Gupta*, a metal layer is stripped back to form a recess (A) in the trench and a capping layer is formed over the metallization to prevent contamination before the next level of metallization. (col. 3, ll. 43-45). In *Gupta,* the capping layer is removed, while leaving the capping in the trench. (col. 3, ll. 47-50). Only in the third embodiment is a CMP process performed, and that CMP process includes only partial removal of only a deposited metal barrier.

The *Ngo, Padhi* and *Gupta* Combination Does Not Suggest Limitations of Claim 1

Applicants respectfully submit that the *Ngo, Padhi* and *Gupta* combination does not disclose or fairly suggest the limitations of claim 1. In particular, the combination of does not disclose or fairly suggest removal of metal residue smeared in an unintended scratch at the surface.

First, in *Ngo* an oxide over metal is formed by a CMP process and that oxide, not the underlying metal, is removed using soft plasma. *Ngo* does not disclose plasma etching a surface to remove metal residue formed in a dielectric substrate. *Padhi* describes that the CMP process is used to remove the metal from the substrate. To the extent that the surface needs any further processing, *Padhi* describes using wet etching techniques to remove oxides, contaminants, and other residual contaminants. Finally, in *Gupta,* a CMP process is used to remove a barrier metal that is coated in the field before the CMP process, which is used only to partially remove the barrier. A blanket etch back is performed to remove the remainder of the barrier.

The *Ngo, Padhi* and *Gupta* combination describes using a CMP process to clean the surface of a substrate, and to the extent further processing may be needed, the combination discloses wet etching techniques to oxides and residual contaminants. Indeed, since *Padhi* discloses that "CMP is suitable for removal of various materials, including metals and dielectric materials," (par. [0063]), the combination does not suggest to one skilled in the art to expose a prepared semiconductor surface to a plasma and inert gas <u>to remove the metal residue</u> smeared in an unintended scratch at the semiconductor surface. To the contrary, the combination discloses using CMP to remove metals and downstream or remote plasma etching only to remove oxides. Therefore, applicants respectfully submit that claim 1 would not be obvious to one skilled in the art over the *Ngo, Padhi* and *Gupta* combination.

<u>Independent claim 10</u>

Independent claim 1 is directed to a method for dry-cleaning a metal residue-filled scratch in a chemical mechanical polished semiconductor surface, where the CMP of the

surface affects the metal residue-filled scratch. In the method, the surface is exposed to a plasma to remove the residue and to form a volatile gas. The plasma is diluted with an inert gas and has a pressure in the range of approximately 0.3 Torr, a gas flow of approximately 100 sccm and a temperature less than approximately 250 °C.

The *Ngo, Padhi* and *Gupta* Combination Does Not Suggest Limitations of Claim 10

Applicants respectfully submit that the *Ngo, Padhi* and *Gupta* combination does not disclose or fairly suggest the limitations of claim 10. As discussed, the *Ngo, Padhi* and *Gupta* combination describes using a CMP process to clean the surface of a substrate, and to the extent further processing may be needed, the combination discloses wet etching techniques to oxides and residual contaminants. Indeed, since *Padhi* discloses that "CMP is suitable for removal of various materials, including metals and dielectric materials," (par. [0063]), the combination does not suggest to one skilled in the art to expose a prepared semiconductor surface to a plasma and inert gas to remove the metal residue smeared in an unintended scratch at the semiconductor surface. To the contrary, the combination discloses using CMP to remove metals and downstream or remote plasma etching only to remove oxides. In addition, none of the cited references describe or fairly suggest exposing a surface to plasma diluted with inert gas having the recited pressure, gas flow and temperature of claim 10. Therefore, applicants respectfully submit that claim 10 would not be obvious to one skilled in the art over the *Ngo, Padhi* and *Gupta* combination.

Dependent Claims

For similar reasons, the *Ngo, Padhi* and *Gupta* combination also fails to disclose or fairly suggest the limitations of claims 2-9 and 11-15. As discussed above, the *Ngo, Padhi*

and *Gupta* combination does not lead to the limitations for independent claims 1 and 10. Therefore, the *Ngo, Padhi* and *Gupta* combination does not disclose or fairly suggest the limitations for claims dependent therefrom. Accordingly, Applicants also respectfully request favorable consideration of claims 2-9 and 11-15.

CONCLUSION

In view of the foregoing amendments and reasons, Applicants respectfully request favorable consideration and earnestly solicit allowance of all pending claims. Inquiries regarding this communication may be directed to the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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